

BUK71/7907-55AIE

TrenchPLUS standard level FET

Rev. 01 — 12 August 2002

Product data

1. Product profile

1.1 Description

N-channel enhancement mode field-effect power transistor in a plastic package using TrenchMOS™ technology, featuring very low on-state resistance, TrenchPLUS current sensing and diodes for ESD protection.

Product availability:

BUK7107-55AIE in SOT426 (D²-PAK)

BUK7907-55AIE in SOT263B (TO-220AB).

1.2 Features

- Integrated current sensor
- ESD protection
- Q101 compliant
- Standard level compatible.

1.3 Applications

- Variable Valve Timing for engines
- Electrical Power Assisted Steering.

1.4 Quick reference data

- $V_{DS} \leq 55$ V
- $I_D \leq 140$ A
- $R_{DSon} = 5.8$ m Ω (typ)
- $I_D/I_{sense} = 500$ (typ).

2. Pinning information

Table 1: Pinning - SOT426 and SOT263B, simplified outline and symbol

Pin	Description	Simplified outline	Symbol
1	gate (g)		
2	I_{sense}		
3	drain (d)		
4	Kelvin source		
5	source (s)		
mb	mounting base; connected to drain (d)		
		SOT426 (D ² -PAK)	SOT263B (TO-220AB)

3. Limiting values

Table 2: Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit	
V_{DS}	drain-source voltage (DC)		-	55	V	
V_{DGS}	drain-gate voltage (DC)	$I_{DG} = 250 \mu\text{A}$	-	55	V	
V_{GS}	gate-source voltage (DC)		-	± 20	V	
I_D	drain current (DC)	$T_{mb} = 25 \text{ }^\circ\text{C}$; $V_{GS} = 10 \text{ V}$; Figure 2 and 3	[1]	-	140	A
			[2]	-	75	A
		$T_{mb} = 100 \text{ }^\circ\text{C}$; $V_{GS} = 10 \text{ V}$; Figure 2	[2]	-	75	A
I_{DM}	peak drain current	$T_{mb} = 25 \text{ }^\circ\text{C}$; pulsed; $t_p \leq 10 \mu\text{s}$; Figure 3	-	560	A	
P_{tot}	total power dissipation	$T_{mb} = 25 \text{ }^\circ\text{C}$; Figure 1	-	272	W	
$I_{GS(CL)}$	gate-source clamping current	continuous	-	10	mA	
		$t_p = 5 \text{ ms}$; $\delta = 0.01$	-	50	mA	
T_{stg}	storage temperature		-55	+175	$^\circ\text{C}$	
T_j	junction temperature		-55	+175	$^\circ\text{C}$	
Source-drain diode						
I_{DR}	reverse drain current	$T_{mb} = 25 \text{ }^\circ\text{C}$	[1]	-	140	A
			[2]	-	75	A
I_{DRM}	peak reverse drain current	$T_{mb} = 25 \text{ }^\circ\text{C}$; pulsed; $t_p \leq 10 \mu\text{s}$	-	560	A	
Avalanche ruggedness						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	unclamped inductive load; $I_D = 68 \text{ A}$; $V_{DS} \leq 55 \text{ V}$; $V_{GS} = 10 \text{ V}$; $R_{GS} = 50 \Omega$; starting $T_j = 25 \text{ }^\circ\text{C}$	-	460	mJ	
Electrostatic Discharge						
V_{esd}	electrostatic discharge voltage; all pins	Human Body Model; $C = 100 \text{ pF}$; $R = 1.5 \text{ k}\Omega$		6	kV	

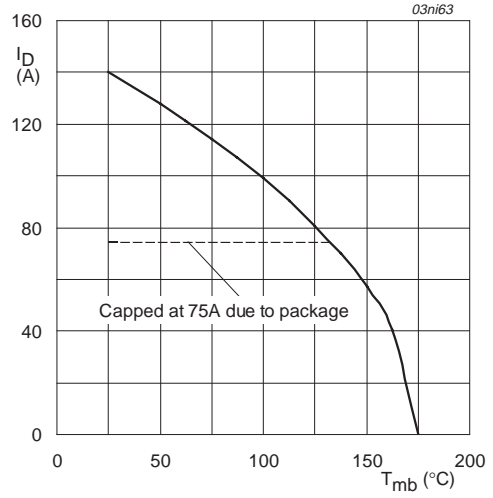
[1] Current is limited by power dissipation chip rating

[2] Continuous current is limited by package.



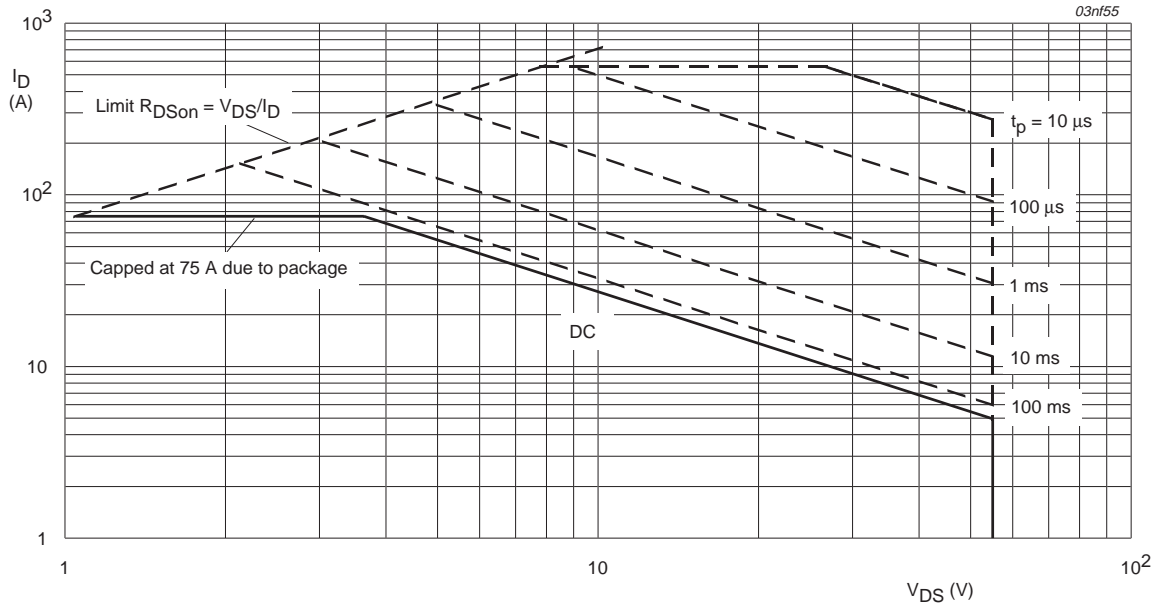
$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}C)}} \times 100\%$$

Fig 1. Normalized total power dissipation as a function of mounting base temperature.



$V_{GS} \geq 10\text{ V}$

Fig 2. Continuous drain current as a function of mounting base temperature.



$T_{mb} = 25^{\circ}C$; I_{DM} single pulse.

Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage.

4. Thermal characteristics

Table 3: Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient					
	SOT263B	vertical in still air	-	60	-	K/W
	SOT426	minimum footprint; mounted on a PCB	-	50	-	K/W
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Figure 4	-	-	0.55	K/W

4.1 Transient thermal impedance

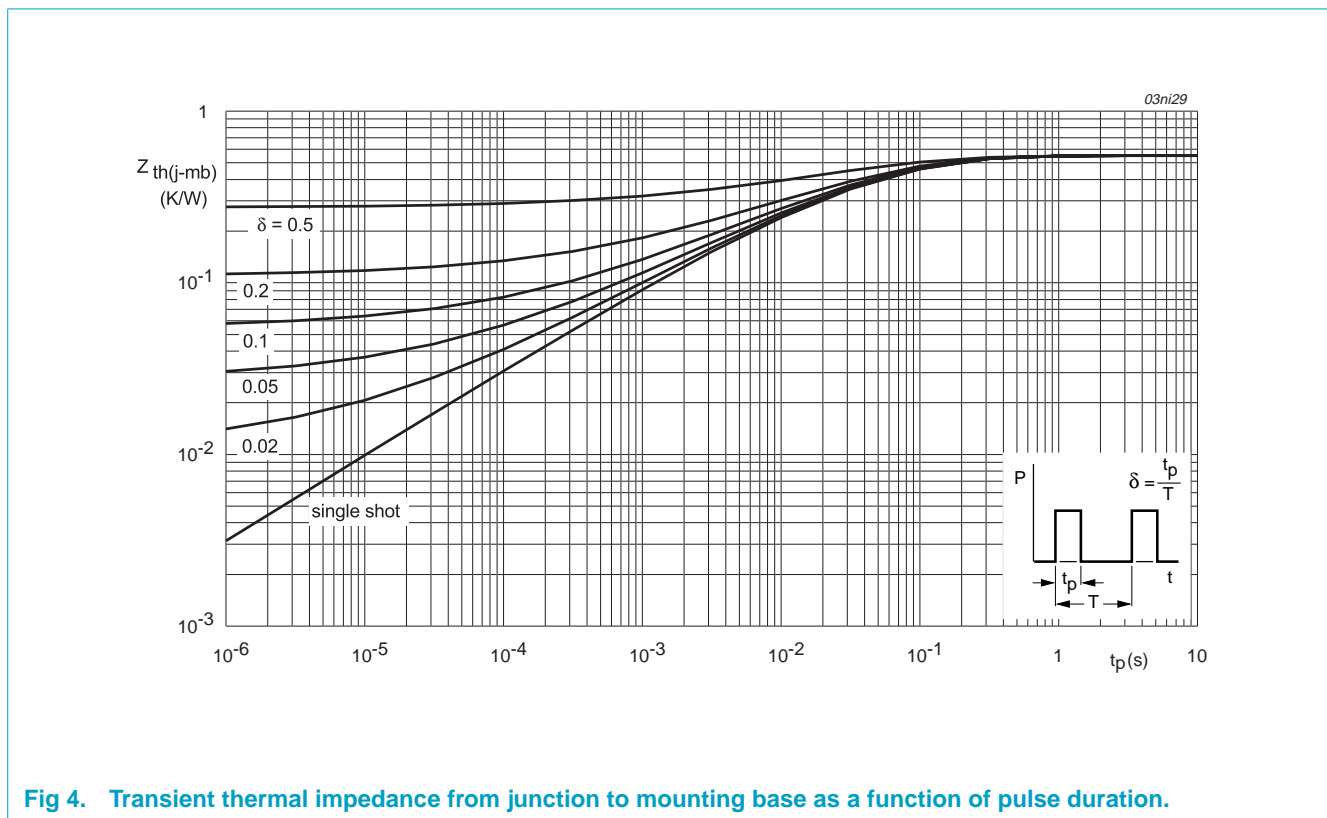


Fig 4. Transient thermal impedance from junction to mounting base as a function of pulse duration.

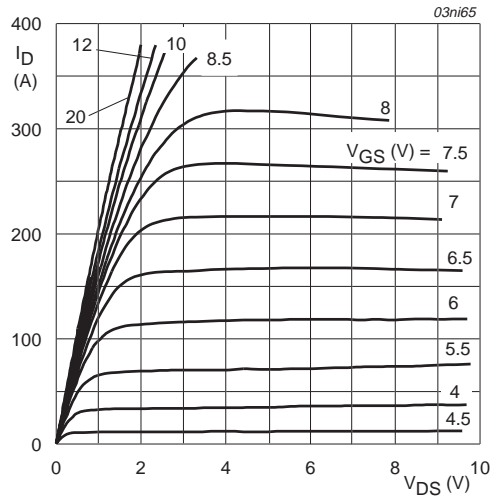
5. Characteristics

Table 4: Characteristics
 $T_j = 25\text{ }^\circ\text{C}$ unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 0.25\text{ mA}$; $V_{GS} = 0\text{ V}$				
		$T_j = 25\text{ }^\circ\text{C}$	55	-	-	V
		$T_j = -55\text{ }^\circ\text{C}$	50	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1\text{ mA}$; $V_{DS} = V_{GS}$; Figure 9				
		$T_j = 25\text{ }^\circ\text{C}$	2	3	4	V
		$T_j = 175\text{ }^\circ\text{C}$	1	-	-	V
		$T_j = -55\text{ }^\circ\text{C}$	-	-	4.4	V
I_{DSS}	drain-source leakage current	$V_{DS} = 55\text{ V}$; $V_{GS} = 0\text{ V}$				
		$T_j = 25\text{ }^\circ\text{C}$	-	0.1	10	μA
		$T_j = 175\text{ }^\circ\text{C}$	-	-	250	μA
$V_{(BR)GSS}$	gate-source breakdown voltage	$I_G = \pm 1\text{ mA}$; $-55\text{ }^\circ\text{C} < T_j < 175\text{ }^\circ\text{C}$	20	22	-	V
I_{GSS}	gate-source leakage current	$V_{GS} = \pm 10\text{ V}$; $V_{DS} = 0\text{ V}$				
		$T_j = 25\text{ }^\circ\text{C}$	-	22	1000	nA
		$T_j = 175\text{ }^\circ\text{C}$	-	-	10	μA
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10\text{ V}$; $I_D = 50\text{ A}$; Figure 7 and 8				
		$T_j = 25\text{ }^\circ\text{C}$	-	5.8	7	m Ω
		$T_j = 175\text{ }^\circ\text{C}$	-	-	14	m Ω
I_D/I_{sense}	ratio of drain current to sense current	$V_{GS} > 10\text{ V}$; $-55\text{ }^\circ\text{C} < T_j < 175\text{ }^\circ\text{C}$	450	500	550	
Dynamic characteristics						
$Q_{g(tot)}$	total gate charge	$V_{GS} = 10\text{ V}$; $V_{DS} = 44\text{ V}$; $I_D = 25\text{ A}$; Figure 14	-	116	-	nC
Q_{gs}	gate-source charge		-	19	-	nC
Q_{gd}	gate-to-drain (Miller) charge		-	50	-	nC
C_{iss}	input capacitance	$V_{GS} = 0\text{ V}$; $V_{DS} = 25\text{ V}$; $f = 1\text{ MHz}$; Figure 12	-	4500	-	pF
C_{oss}	output capacitance		-	960	-	pF
C_{rss}	reverse transfer capacitance		-	510	-	pF
$t_{d(on)}$	turn-on delay time	$V_{DS} = 30\text{ V}$; $R_L = 1.2\text{ }\Omega$;	-	36	-	ns
t_r	rise time	$V_{GS} = 10\text{ V}$; $R_G = 10\text{ }\Omega$	-	115	-	ns
$t_{d(off)}$	turn-off delay time		-	159	-	ns
t_f	fall time		-	111	-	ns
L_d	internal drain inductance	from upper edge of drain mounting base to center of die	-	2.5	-	nH
L_s	internal source inductance	from source lead to source bond pad	-	7.5	-	nH

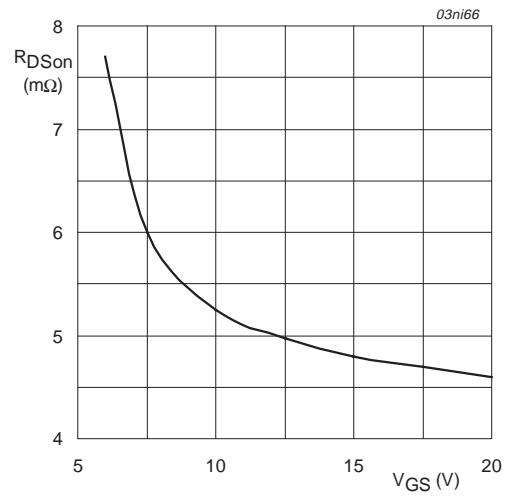
Table 4: Characteristics...continued*T_j = 25 °C unless otherwise specified.*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Source-drain diode						
V _{SD}	source-drain (diode forward) voltage	I _S = 25 A; V _{GS} = 0 V; Figure 16	-	0.85	1.2	V
t _{rr}	reverse recovery time	I _S = 20 A; dI _S /dt = -100 A/μs	-	80	-	ns
Q _r	recovered charge	V _{GS} = -10 V; V _{DS} = 30 V	-	200	-	nC



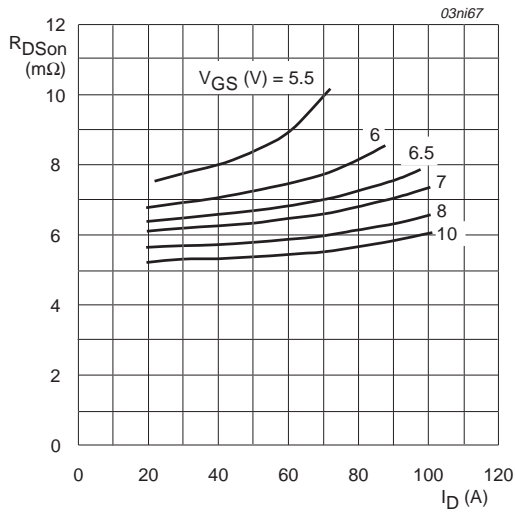
$T_j = 25\text{ }^\circ\text{C}$; $t_p = 300\text{ }\mu\text{s}$

Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values.



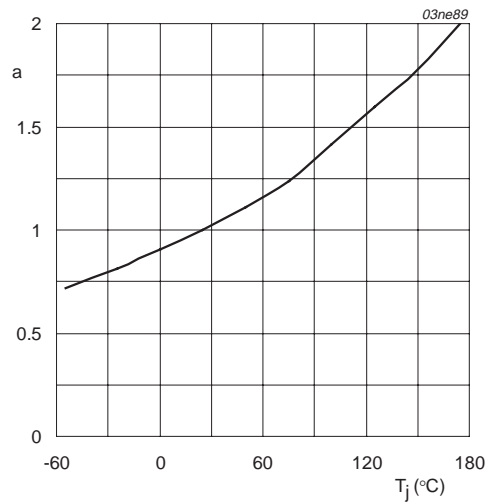
$T_j = 25\text{ }^\circ\text{C}$; $I_D = 50\text{ A}$

Fig 6. Drain-source on-state resistance as a function of gate-source voltage; typical values.



$T_j = 25\text{ }^\circ\text{C}$; $t_p = 300\text{ }\mu\text{s}$

Fig 7. Drain-source on-state resistance as a function of drain current; typical values.



$$a = \frac{R_{DSon}}{R_{DSon(25^\circ\text{C})}}$$

Fig 8. Normalized drain-source on-state resistance factor as a function of junction temperature.



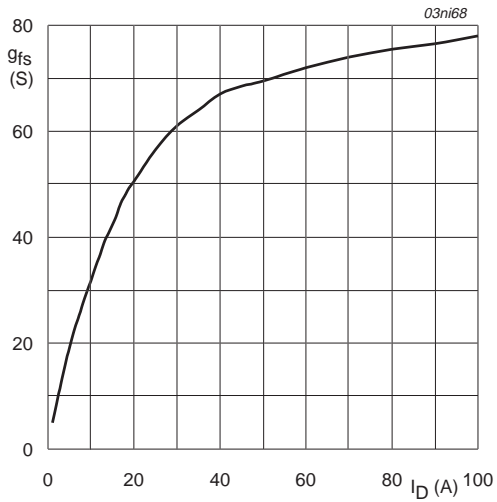
$I_D = 1 \text{ mA}; V_{DS} = V_{GS}$

Fig 9. Gate-source threshold voltage as a function of junction temperature.



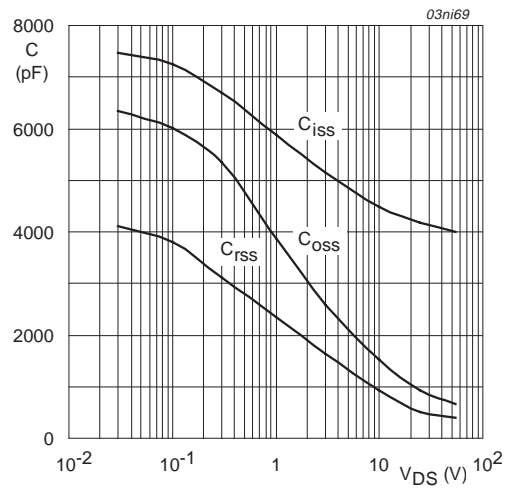
$T_j = 25 \text{ }^\circ\text{C}; V_{DS} = V_{GS}$

Fig 10. Sub-threshold drain current as a function of gate-source voltage.



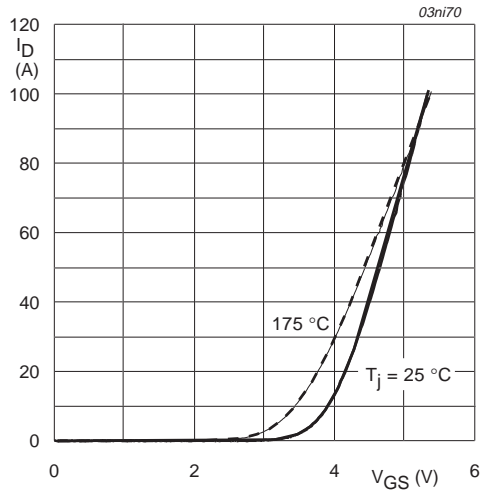
$T_j = 25 \text{ }^\circ\text{C}; V_{DS} = 25 \text{ V}$

Fig 11. Forward transconductance as a function of drain current; typical values.



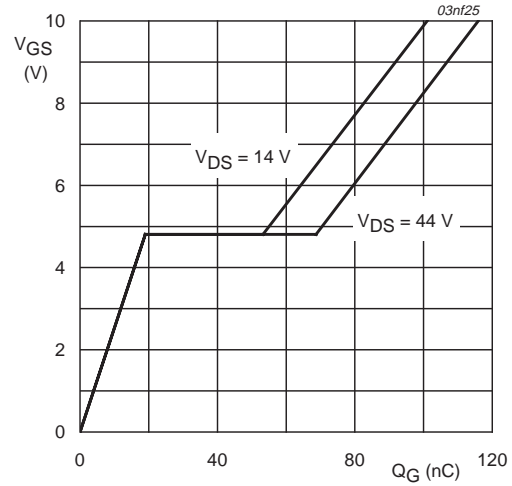
$V_{GS} = 0 \text{ V}; f = 1 \text{ MHz}$

Fig 12. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values.



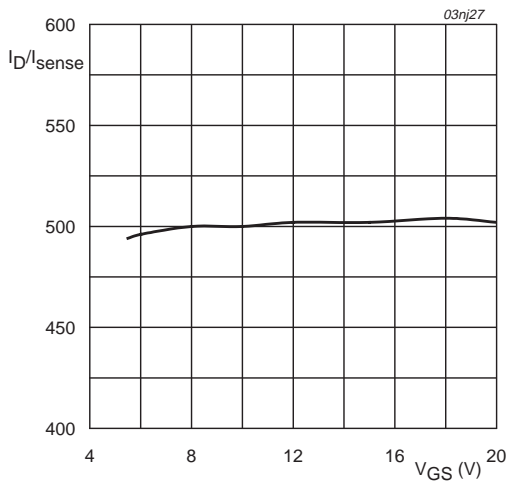
$V_{DS} = 25 \text{ V}$

Fig 13. Transfer characteristics: drain current as a function of gate-source voltage; typical values.



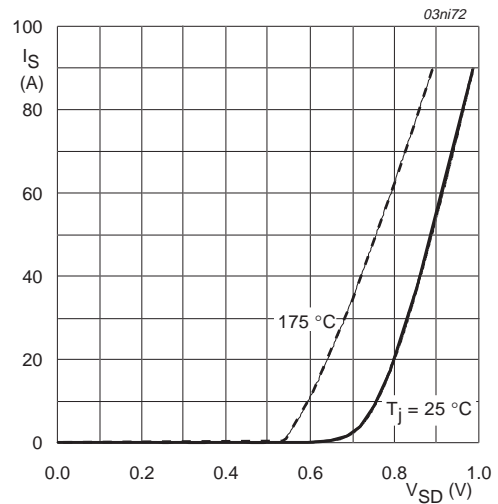
$T_j = 25 \text{ °C}; I_D = 25 \text{ A}$

Fig 14. Gate-source voltage as a function of turn-on gate charge; typical values.



$I_D = 25 \text{ A}$

Fig 15. Drain-sense current ratio as a function of gate-source voltage; typical values.



$V_{GS} = 0 \text{ V}$

Fig 16. Reverse diode current as a function of reverse diode voltage; typical values.

6. Package outline

Plastic single-ended surface mounted package (Philips version of D²-PAK); 5 leads (one lead cropped)

SOT426

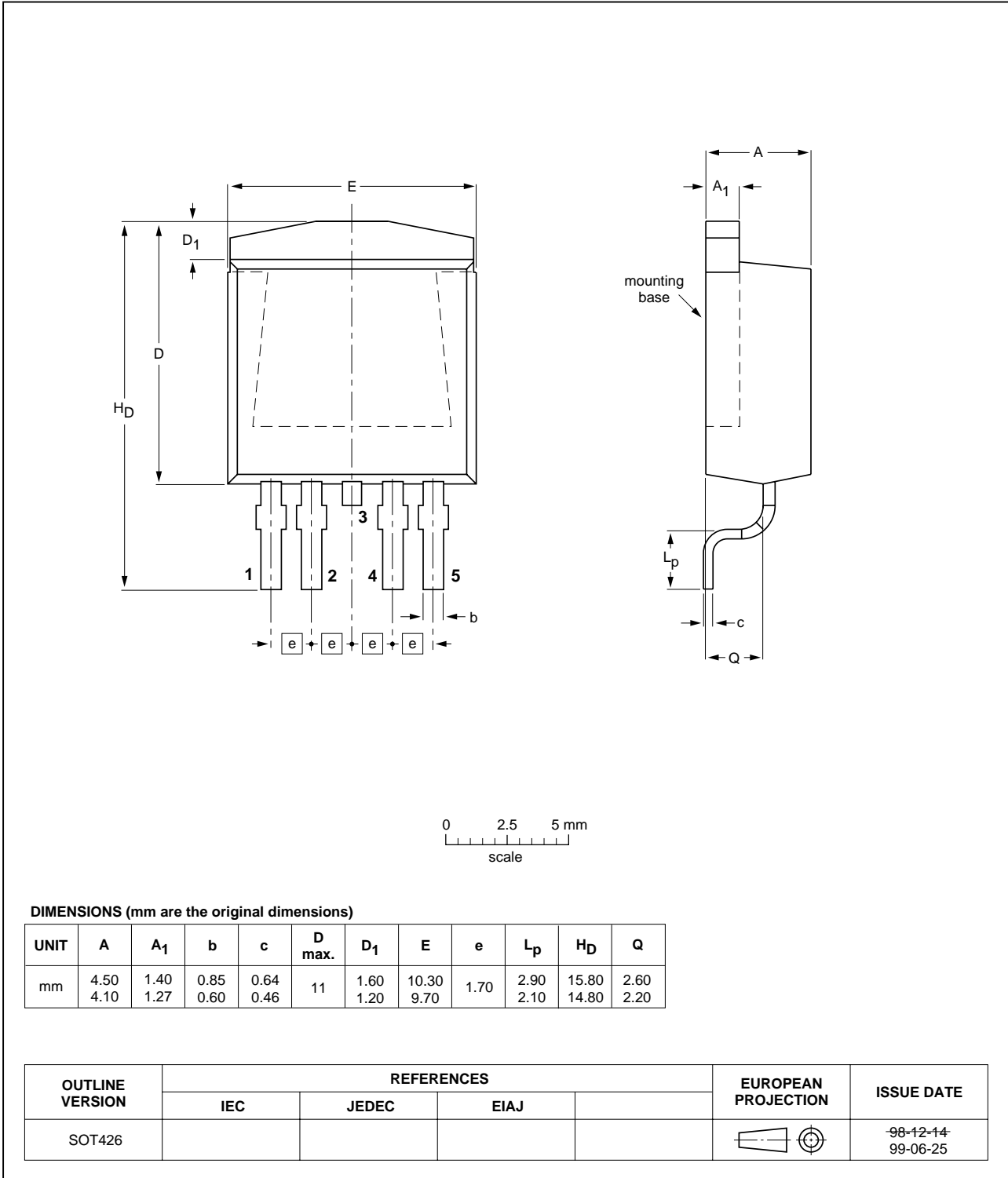


Fig 17. SOT426 (D²-PAK).

Plastic single-ended package; heatsink mounted; 1 mounting hole; 5-lead TO-220

SOT263B

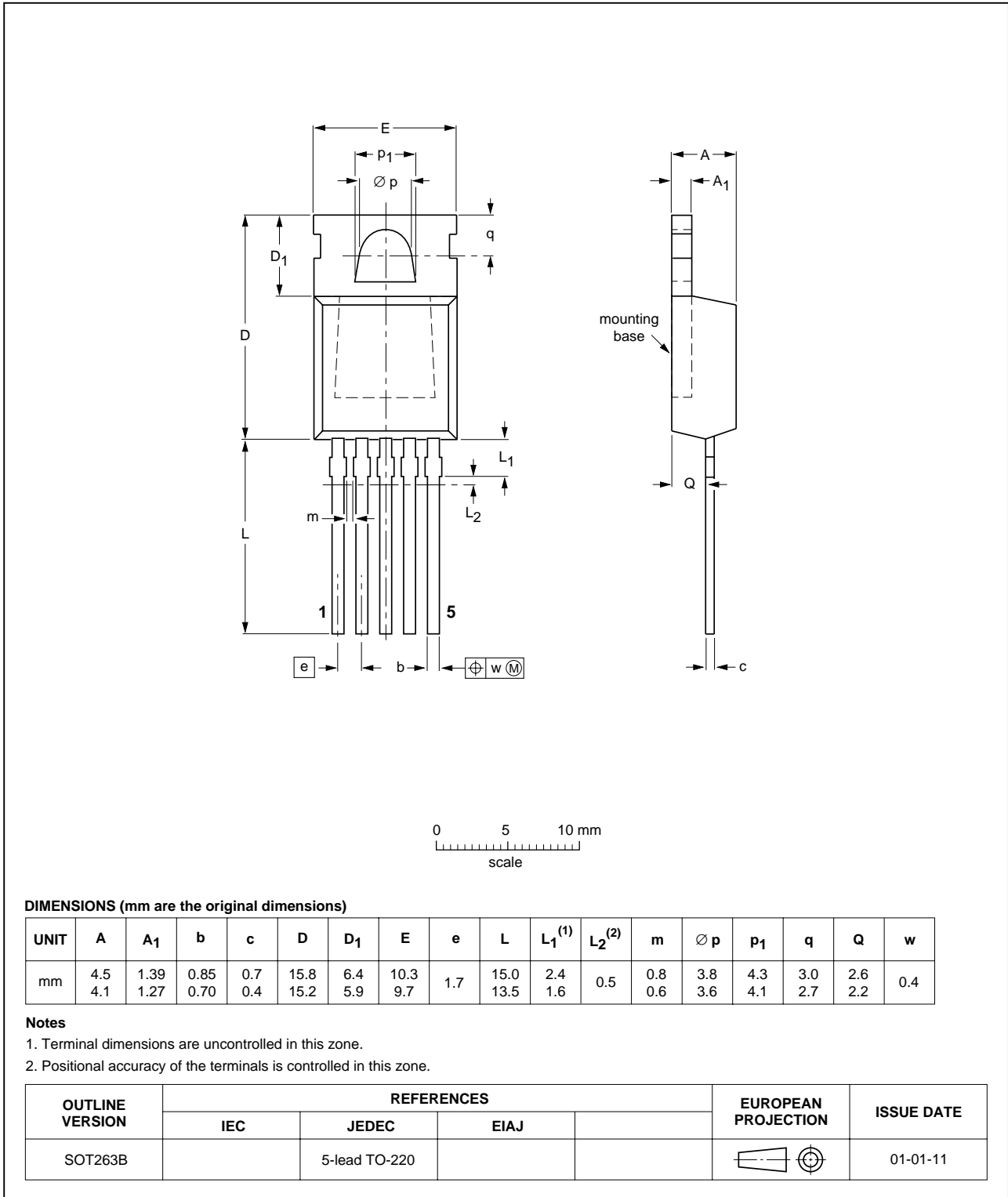
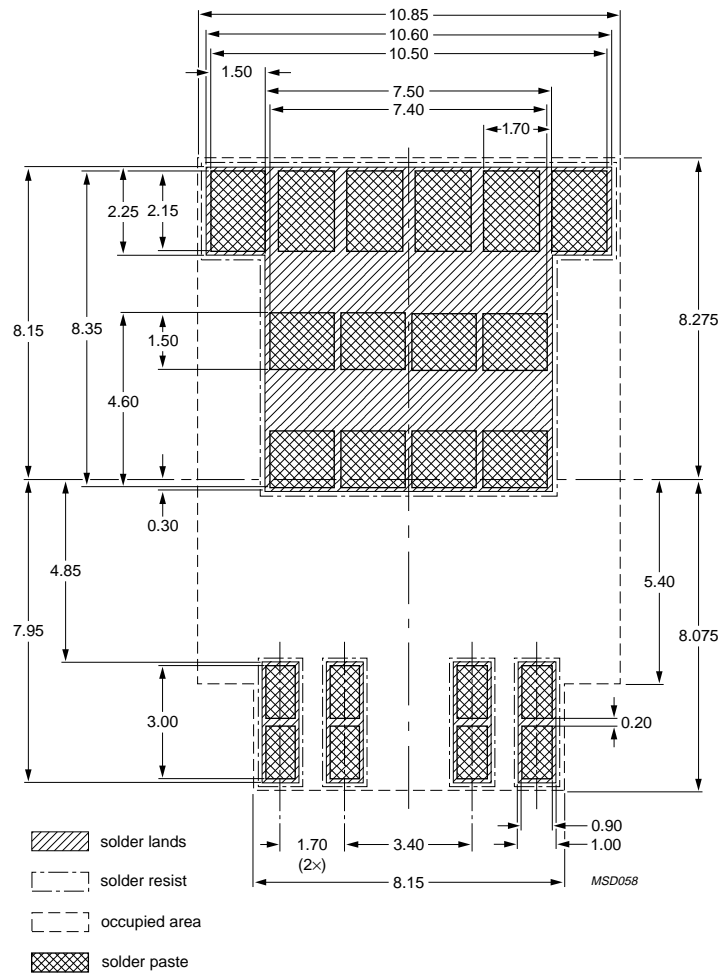


Fig 18. SOT263B (TO-220AB).

7. Soldering



Dimensions in mm.

Fig 19. Reflow soldering footprint for SOT426.

8. Revision history

Table 5: Revision history

Rev	Date	CPCN	Description
01	20020812	-	Product data; initial version

9. Data sheet status

Data sheet status ^[1]	Product status ^[2]	Definition
Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
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[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL <http://www.semiconductors.philips.com>.

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